

High performance of potassium n-doped carbon nanotube field-effect transistors

M. Radosavljević^a, J. Appenzeller^b, and Ph. Avouris^c

IBM Research Division, T. J. Watson Research Center, Yorktown Heights, New York 10598, USA

J. Knoch

Institut für Schichten und Grenzflächen, Forschungszentrum Jülich, D-52425 Jülich, Germany

(February 2, 2008)

We describe a robust technique for the fabrication of high performance vertically scaled n-doped field-effect transistors from large band gap carbon nanotubes. These devices have a tunable threshold voltage in the technologically relevant range ($-1.3 \text{ V} \leq V_{\text{th}} \leq 0.5 \text{ V}$) and can carry up to $5-6 \mu\text{A}$ of current in the on-state. We achieve such performance by exposure to potassium (K) vapor and device annealing in high vacuum. The treatment has a two-fold effect to: (i) controllably shift V_{th} toward negative gate biases via bulk doping of the nanotube (up to about $0.6 e^-/\text{nm}$), and (ii) increase the on-current by 1-2 orders of magnitude. This current enhancement is achieved by lowering external device resistance due to more intimate contact between K metal and doped nanotube channel in addition to potential reduction of the Schottky barrier height at the contact.

Recent fabrication of complimentary logic gates based on carbon nanotube transistors (CNFETs) has intensified the interest in nanoelectronic applications for these materials. [1,2] These initial gates showed performance which was limited by the device characteristics of the constituent CNFETs. In the interim, many more improvements have been made on p-CNFETs than on complimentary n-type transistors. [3–5] This is mostly because p-CNFETs are readily available under ambient conditions due to oxygen induced dipoles at the interface between the metal electrode and the CN. [6] In contrast, n-CNFETs require controlled environment, either by doping with electropositive elements, such as potassium (K) metal [7,8] or by annealing/out gassing the oxygen at the contacts. [4,9] While these two methods use very different physical mechanisms to achieve n-CNFETs, neither has been successful at approaching the performance (i.e. on- and off-states as well as subthreshold slope) of best p-CNFETs.

In this letter we report on a technique that allows reproducible optimization of device characteristics by (i) increasing the charge density in the channel and (ii) lowering of the external series resistance. After outlining the experimental details of the technique which consists of a combination of K-doping and device annealing, we discuss the performance gains in both the on- and the off-states. Our n-CNFETs show on-currents ($\sim 5-6 \mu\text{A}$, Ref. [10]) which rival those of the best p-CNFETs produced to date [3] from small diameter CNs as discussed below. [11] In the off-state, we obtain a value of subthreshold swing (S) $\leq 150 \text{ mV/decade}$ due to good electrostatic control [12] by the gate field (oxide thickness, $t_{\text{ox}} = 5 \text{ nm}$). Both of these observations are in agreement with expectations based on the symmetric band structure and identical electron and hole masses in CNs, [13] and they remain unchanged as the device threshold voltage is tuned over a technologically relevant gate range, $-1.3 \text{ V} \leq V_{\text{th}} \leq 0.5 \text{ V}$ (corresponding to a charge density

increase from nearly zero up to about $0.6 e^-/\text{nm}$.)

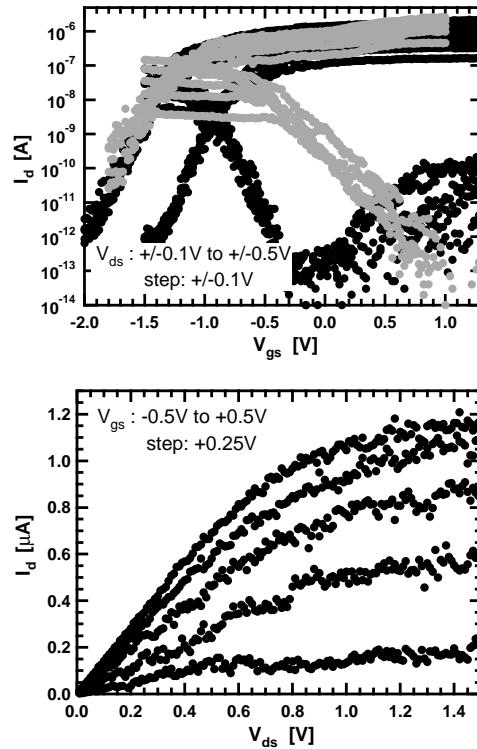


FIG. 1. (a) Transfer characteristics showing conversion of two different CNFETs (in black and grey) from p- to high performance n-type devices through exposure to K vapor and vacuum annealing. (b) Output characteristics at an intermediate stage of conversion (black) with transconductance in excess of $1 \mu\text{S}$ at $V_{\text{ds}} = +1.5 \text{ V}$.

Finally, we discuss the connection of the observed changes in the device characteristics to the cycle of K exposure/annealing, focusing in particular on the effect of doping of the CN channel, and lowering of the exter-

nal device resistance due to formation of a more intimate contact between potassium and the nanotube.

For this work, we have fabricated CNFETs with titanium source and drain electrodes separated by 300-400 nm and Si-backgate ($t_{\text{ox}} = 5 \text{ nm}$) as described elsewhere. [14] Specifically, we focus on rather small diameter nanotubes ($1.4 \pm 0.2 \text{ nm}$) which exhibit band gaps of around 0.6-0.7 eV. [11] These semiconducting CNs are sufficiently similar to silicon in terms of their band gap size that they are suitable for ultimately scaled transistor applications. All transport data are acquired at negative (positive) drain bias (V_{ds}) for p-(n-)CNFETs at room temperature in a high vacuum system (base pressure 10^{-7} Torr .) Doping is done in-situ using a resistive potassium source. [8,9] We use short K-deposition steps (1-2 min) followed by brief (30 min) anneals at temperatures between 120-170 °C. Annealing temperature in this range significantly increases the mobility of K on the substrate and allows quasi-uniform distribution on the nanotube, as has been shown in the case of other fullerenes. [15] After each device has been exposed to some number of doping/annealing cycles (typically a *total* of 10-15 min of K vapor and 4-16 hours of annealing), it arrives at a final state where performance can not be improved with further processing. Additional benefit of annealing after deposition is that it prevents gross overcoating of the nanotube, as well as the area between the source and the drain with potassium. [7] The observed improvement cannot be achieved by doping alone which only shifts the threshold voltage toward negative gate values (V_{gs}) without any increase in electron current (data not shown).

Next we compare the performance of the as-prepared CNFETs with the device characteristics resulting following the exposure to K-doping and annealing. Figure 1(a) shows initial and final transfer characteristics (I_{d} vs. V_{gs}) of two different devices converted in two different runs. The final devices show two clearly apparent differences compared to the as-prepared CNFET: (i) the V_{th} for electron conduction shifts from about 0.5 V in (nearly) intrinsic CNFET to -1.3 V , and (ii) the on-current for electrons is increased by 3-4 orders of magnitude compared to the initial electron current and is 10-100 times higher than initially more pronounced hole current. This second effect is a direct consequence of the annealing of the device and constitutes the main experimental finding of this work.

Beyond the outlined changes, our CNFETs behave as excellent depletion mode n-type transistors. In particular, the inverse subthreshold slope, $S = dV_{\text{gs}}/d(\log I_{\text{d}}) \leq 150 \text{ mV/decade}$ approaches the thermal limit. This is because of the improved electrostatics due to the thin 5 nm oxide which affords great control over the nanotube bands such that tunneling through the SB [12,16,17] proceeds with nearly perfect transmission. [18] Throughout the K exposure and annealing, the device maintains a steep subthreshold slope and a large on-off ratio 5-6 (or

ders of magnitude) even at $V_{\text{ds}} \sim 1.0 \text{ V}$, which is due to the small diameter and correspondingly rather large band gap of our nanotubes. [18,19] Another potential advantage of CNFETs if compared to Si-based devices is the predicted identical performance of p- and n-transistors due to same values for hole and electron effective masses. Figure 1(b) shows the output characteristic (I_{d} vs. V_{ds}) of the improved n-CNFET in the intermediate conversion in Fig. 1(a). Even at this stage currents in excess of $1 \mu\text{A}$ are driven through the device, corresponding to a large transconductance $g_{\text{m}} = dI_{\text{d}}/dV_{\text{gs}} \sim 1 \mu\text{S}$. Further K exposure and annealing results in improvement by about a factor of 3-5 in g_{m} . [10] These values are comparable to the very best small diameter p-CNFETs, [3] in line with the expectations based on the band structure. All these observations together suggest that device performance can be optimized in *both* on- and off-states without sacrificing the tunability of V_{th} .

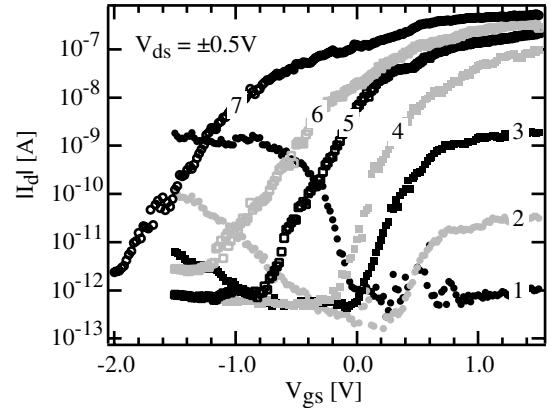


FIG. 2. Stepwise conversion and improvement of a CNFET. Initial p-type curve (#1) is followed by one with ambipolar characteristics (#2) due to vacuum annealing. Consecutive doping and annealing steps (#3-#7) gradually transform the device into an n-CNFET by increasing the on-current and shifting the threshold voltage to more negative values.

Given these promising device characteristics, we would like to understand the mechanism of this improvement by looking at a stepwise doping and annealing cycle such as shown in Figure 2. The initial p-CNFET (curve #1) is converted to an ambipolar device (curve #2) by an overnight vacuum anneal at 170 °C. [9] Curves #3-7 show 5 consecutive short doping/annealing steps all of which exhibit *both* a shift in the threshold voltage and an increase in the on-current compared to previous characteristic. This implies that potassium exposure and heating treatment are responsible for both effects. However, if potassium only transfers charge to the nanotube by chemically doping the body of the nanotube (device bulk), this would explain the threshold voltage shift but not the increase in on-current. For this reason, we have to conclude that the observed changes are produced by a

combination of bulk doping and improved injection from the source electrode into the CNFET. In the following we consider each aspect independently.

In our previous work we have focused on the off-state of nanotube transistors [12,17]. Here the emphasis is on how the on-current I_d^{on} of a CNFET is affected by potassium exposure and annealing treatment. First, we evaluate the performance of the initial, undoped device. $|I_d^{\text{on}}|$ is typically in the nA range [see Figs. 1(a) and 2] at drain voltages $V_{ds} = -0.5$ V. In comparison with the *expected* response from self-consistent quantum mechanical simulations on the performance of Schottky barrier (SB) CNFETs [20] this current is at least one order of magnitude too small - see Fig. 3. This statement is true no matter what Schottky barrier height Φ_B is assumed for a gate oxide thickness of $t_{\text{ox}} = 5$ nm. Other groups have also pointed out that $|I_d^{\text{on}}|$ becomes progressively less affected by Φ_B the stronger the gate impact (e.g. the thinner the gate dielectric). [18] At the same time the n-type devices after K-deposition show regularly on-currents that are in the micro-amps range as expected for our device geometry. Since the increase in on-current between devices before and after K-doping cannot be explained as a result of a barrier lowering *and* $|I_d^{\text{on}}|$ is always too low for the initial CNFETs, we conclude that an additional contact resistance is present before K-deposition. [21]

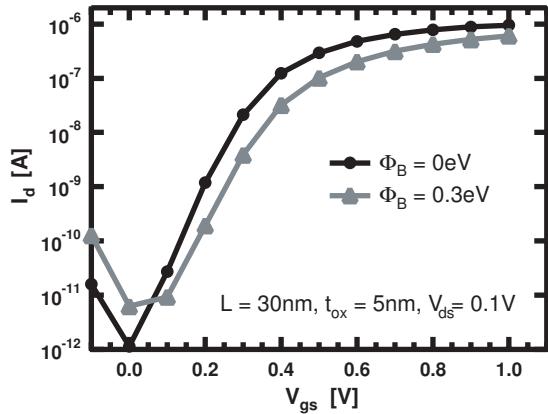


FIG. 3. Transfer characteristics for different SB heights of a typical small diameter nanotube in our device geometry modelled by a fully self-consistent, quantum mechanical simulations (see Ref. [20]). It is evident that the on-current is initially (at midgap line-up) much higher than in the experiment and that it increases by less than an order of magnitude with lowering of the SB height.

In order to *consistently* explain our experimental observations we have to assume that this extra series resistance limits the device performance in the *on-state* prior to the potassium treatment and has vanished or substantially decreased afterwards. This observation is in agreement with the reports that the metal/nanotube contact resistance for metals having similar work functions can be substantially different. [5] It is believed that this ef-

fect is related to the varying ability of different metals to wet the nanotube surface. [22] Our results indicate that the intimacy between the contacting metal and the nanotube changes when the titanium/nanotube interface is replaced by a potassium/nanotube contact as is the case after K-doping and annealing. It should be noted that this gate field-independent contact resistance is *NOT* a replacement for the formerly introduced Schottky barrier (SB) model. SBs have to be assumed to explain in particular the transistor *off-state* characteristics. [12,17] Instead, our findings here suggest that *in addition* a field independent parasitic resistance has to be taken into account using certain metal contacts to explain the transistor *on-state*.

Next we discuss the correspondence between the shift in the Fermi level of the CN due to K-deposition and the movement of the V_{th} compared to an undoped device. Since the gate dielectric is quite thin ($t_{\text{ox}} = 5$ nm) we can to first order estimate the change in the Fermi level, at any value of SB height, to be the same as the change in the threshold voltage: $\Delta E_F = q\Delta V_{\text{th}}$. In Fig. 2, the Fermi level shifts by about 1 eV from the intrinsic (#2) to the fully doped curve (#7), implying that it has moved ~ 500 meV into the conduction band. The inferred doping level is quite a bit higher than in bulk Si where the highest doping is to ~ 100 meV above the conduction band edge (and ~ 30 meV below the valence band edge) due in part to ineffective screening in one-dimension (1D).

Finally, we try to use the estimated Fermi level position to extract the actual linear charge density transferred from K vapor by computing the 1D density of states for a parabolic band. By accounting for both bands and spin degrees of freedom in a CN and omitting Fermi distribution function to simplify the integral we obtain $n_{1d} = (\sqrt{8m^*(E_F - E_c)})/(\pi\hbar)$, where m^* is the effective mass, and $(E_F - E_c)$ is the position of the Fermi level compared to the band edge (≤ 500 meV in our experiment). Substituting numerical values $n_{1d} \sim 3.2 \text{ nm}^{-1} \sqrt{(m^*/m_0)(E_F - E_c)[\text{eV}]}$ and given $(m^*/m_0) \sim 0.06$ for CNs of this diameter, we obtain $n_{1d} \sim 0.6 \text{ nm}^{-1}$. This is indeed a high linear doping density corresponding to a bulk density $n_{3D} \sim 10^{20} \text{ cm}^{-3}$. As there are approximately 180 carbon atoms/nm of length in small diameter CNs, this linear density converts to stoichiometric formula of KC_{300} assuming that each K atom donates one full electron. [23] The doping level is similar to previously computed densities in other doped CNFETs, [7] but far below the charge transfer inferred in optical experiments. [24]

In summary, we have developed a technique which reproducibly yields high performance (on-current 5-6 μA) n-CNFETs by utilizing K-doping/annealing to: (i) increase the charge density in the channel (up to $0.6 e^-/\text{nm}$), (ii) reduce external resistances (and likely SB height) in the device. Doping/annealing cycles give

the ability to tune the threshold voltage over a wide, technologically relevant range ($-1.3 \text{ V} \leq V_{\text{th}} \leq 0.5 \text{ V}$). Our CNFETs benefit from using large band gap/small diameter nanotubes and vertical scaling to ensure excellent off-state, switching and subthreshold swing ($S \leq 150 \text{ mV/decade}$). Together, these features make the devices reported here on par with *any* of the best p-CNFETs fabricated to date, [3–5] and most appropriate for integration into nanotube-based complimentary logic gates.

We wish to thank J. Buccignano for e-beam exposures, and B. Ek for expert technical assistance.

^a Present address: Intel Corporation, Component Research, 5200 NE Elam Young Parkway, RA3-252, Hillsboro, OR 97124

^b Electronic address: joerga@us.ibm.com

^c Electronic address: avouris@us.ibm.com

[1] V. Derycke, R. Martel, J. Appenzeller, and Ph. Avouris, *Nano Lett.* **1**, 453 (2001).

[2] X. Liu, C. Lee, C. Zhou, and J. Han, *Appl. Phys. Lett.* **79**, 3329 (2001).

[3] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and Ph. Avouris, *Appl. Phys. Lett.* **80**, 3817 (2002).

[4] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom, and H. J. Dai, *Nature Mat.* **1**, 241 (2002).

[5] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, *Nature* **424**, 654 (2003).

[6] X. Cui, M. Freitag, R. Martel, L. Brus, and Ph. Avouris, *Nano Lett.* **3**, 783 (2003).

[7] M. Bockrath, J. Hone, A. Zettl, P. L. McEuen, A. G. Rinzler and R. E. Smalley, *Phys. Rev. B* **61**, 10606(R) (2000).

[8] J. Kong, C. Zhou, E. Yenilmez, and H. J. Dai, *Appl. Phys. Lett.* **77**, 3977 (2000).

[9] V. Derycke, R. Martel, J. Appenzeller, and Ph. Avouris, *Appl. Phys. Lett.* **80**, 2773 (2002).

[10] It is worth noting that this magnitude of on-current in K-doped n-CNFETs has been previously reported on devices with thicker gate oxide and unoptimized subthreshold swing. [1]

[11] The nanotubes were grown by laser ablation as described in A. Thess *et al.*, *Science* **273**, 483 (1996).

[12] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S. J. Wind, and Ph. Avouris, *Phys. Rev. Lett.* **89**, 126801 (2002).

[13] The prediction of identical electron and hole masses is made based on the band structure of graphene, see e.g. M. S. Dresselhaus, G. Dresselhaus, and Ph. Avouris (eds.), *Carbon nanotubes: synthesis, structure, properties and applications*. (Springer-Verlag, Berlin, Germany, 2001).

[14] S. J. Wind, M. Radosavljević, J. Appenzeller, and Ph. Avouris, *J. Vac. Sci. and Technol. B* **21**, 2856 (2003).

[15] D. M. Poirier, T. R. Ohno, G. H. Kroll, Y. Chen, P. J. Benning, J. H. Weaver, L. P. F. Chibante, R. E. Smalley, *Science* **253**, 646 (1991).

[16] R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K. K. Chan, J. Tersoff, and Ph. Avouris, *Phys. Rev. Lett.* **87**, 256805 (2001).

[17] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and Ph. Avouris, *Phys. Rev. Lett.* **89**, 106801 (2002).

[18] J. Guo, S. Datta, and M. Lundstrom, *cond-mat/0306199*.

[19] M. Radosavljević, S. Heinze, J. Tersoff, and Ph. Avouris, *Appl. Phys. Lett.* **83**, 2435 (2003).

[20] J. Knoch, S. Mantl, and J. Appenzeller, submitted.

[21] While a change in SB height (see Fig. 3) does not account for the observed increase in on-current, it is likely that it indeed occurs through our treatment. However, since the barrier lowering results in a minimal on-current increase in these scaled devices [20], the change in SB height must be assessed using temperature dependent measurements as demonstrated in J. Appenzeller, M. Radosavljević, J. Knoch, and Ph. Avouris, *Phys. Rev. Lett.* **92**, 048301 (2004).

[22] Y. Zhang and H. Dai, *Appl. Phys. Lett.* **77**, 3015 (2000).

[23] C. Jo, C. Kim, and Y. H. Lee, *Phys. Rev. B* **65**, 035420 (2002).

[24] See e.g. S. Kazaoui, N. Minami, R. Jacquemin, H. Kataura, and Y. Achiba, *Phys. Rev. B* **60**, 13339 (1999). These studies support our conclusions that most of the V_{th} shift occurs due to direct charge transfer between K ions and CNFET, rather than through an additional gating component produced by the electrostatic effects of the K^+ ions lying on the device surface.